2016 1st International Electrical Engineering Congress (IEEC 2016)
May. 13-14, 2016 in IEP Centre, Karachi, Pakistan

Evaluation of SilTerra's 130nm CMOS Radio Frequency Integrated Circuit (RF IC) Technology for Power Amplifier Design

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Abstract: Research in the field of RF IC design is often hindered by the cost of IC fabrication especially in third-world countries where budgets are quite modest. SilTerra, a cost-effective Malaysian IC foundry, has the potential to accelerate R&D activities by making IC fabrication feasible for many. Hence, this research aims to evaluate SilTerra's 130nm CMOS RF IC technology by employing it for the design of a fully-integrated Class-E Power Amplifier (PA) with an aim to obtain maximum efficiency and output power while keeping chip size to a minimum. The simulation results verify that the technology is capable of being employed for cutting-edge R&D projects. The PA design achieves 29.2 dBm output power with 47.1% Power Added Efficiency (PAE) at 1.8GHz. However, after back-annotation of layout parasitic values, it achieves 26.8 dBm output power with 38.9% PAE with a chip size of 1mm^2.
Keywords: Radio-Frequency Integrated Circuits (RF IC), CMOS Power Amplifier, Class-E, SilTerra.

I. INTRODUCTION

The quest for designing power-efficient wireless devices often boils down to finding ways of improving the efficiency of RF Power Amplifiers (PAs). This is because PA is the most power hungry module of the RF frontend and its efficiency largely determines the efficiency of the transceiver. Thus, extensive research is being conducted globally in the field of RF Power Amplifiers in order to fulfill the ever-increasing demands of wireless data transfer.

CMOS has been the technology of choice for digital circuits for decades. However, it was not considered suitable for RF front end implementations. These applications traditionally employed GaAs, SiGe and other high speed bipolar technologies. However, with the scaling of CMOS transistors, the sub-micron channel length increased f_t into tens of gigahertz range making it possible to operate CMOS circuits into RF and microwave range. Thus, CMOS is now used for RF applications as well. In fact, it is the most cost-effective solution as it gives performance comparable to SiGe and other exotic technologies, while being considerably cheaper.

Switch-mode PAs, especially Class-E [1, 2], are the most power efficient PAs due to Zero Voltage Switching conditions which significantly minimize power losses.

Although they are not suitable for applications having stringent requirements of linearity, they indeed offer a viable solution for modulation schemes having constant envelope signals. Further using linearization techniques, they can be used for other modulation schemes as well.

In this paper, we describe a fully integrated Differential Cascode Class-E PA designed using SilTerra's 130nm CMOS RF IC technology in order to provide a justifiable evaluation of adopting SilTerra for PA designs. The driving stage and output balun is integrated on-chip with the main amplifying stage. The entire design process which entails schematic entry, layout design, physical verification, parasitic extraction and circuit simulation has been carried out using Cadence Virtuoso environment. Further, in order to perform a judicious evaluation, features of SilTerra's technology are compared with those provided by IBM's equivalent technology as well.

The paper is organized as follows: Section II discusses the PA schematic design, the problems faced during implementation and the strategies used for obtaining optimum simulation results. Section III describes the layout design and the unique features available in SilTerra Process Development Kit (PDK). Section IV presents the results and Section V draws the conclusion.

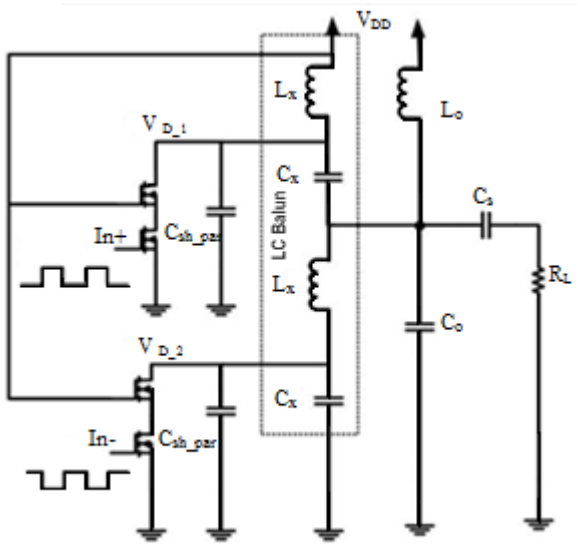


Figure 1 Schematic of differential Cascode Class-E PA with LC tank.

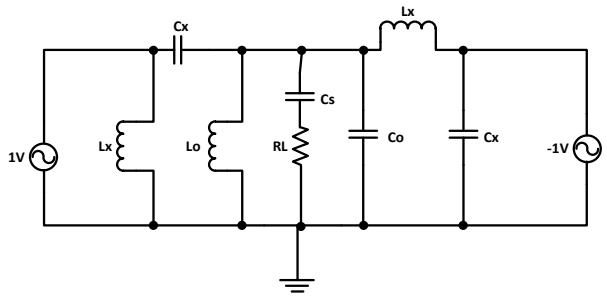


Figure 2 Test circuit schematic

II. SCHEMATIC DESIGN

A. Differential Cascode Class-E PA:

Fig. 1 shows schematic of the Differential Cascode Class-E PA along with an LC Balun which is used for obtaining a single-ended output. The balun, consisting of L_X and C_X, also acts as an impedance transformation network as well as a resonant filter.

In order to achieve high power output from the PA, supply voltage needs to be increased. However, high supply voltage causes stress on the device which may lead to secondary effects such as oxide breakdown, hot carrier effect, velocity saturation etc. Thus, a cascode configuration is used in order to increase the supply voltage while avoiding stress on the transistors.

Bulk of the common gate device has been tied with its source instead of being grounded. This prevents power losses due to slow charging of the parasitic capacitances existing between the source of common gate device and ground. This approach is known as "Charging Acceleration Technique (CAT)" [3].

Differential configuration has been employed for the PA as its power output is twice that of a single-ended design for the same load resistance. Moreover, it suppresses the even harmonics at the output relieving the task of the output filter to some extent.

To obtain high power output, transistors with large widths are required which can allow high current. However, SilTerra PDK does not allow a single transistor to have a width of more than 640 µm. Hence, multiple transistors are connected in parallel in order to achieve the required transistor widths.

As shown in Fig. 1, an additional inductor (L_0) is used in order to provide a DC path for the bottom arm of the differential PA. However, due to a finite inductance, it interferes with the frequency response of the output network. Hence a capacitor (C_0) is added which is tuned so as to resonate along with L_0, thus cancelling its effect on the output network. This combination of L_0 and C_0 is termed as an LC tank. The series capacitor C_S provides the necessary phase shift required for Class-E operation.

The design provides satisfactory simulation results with ideal passive components. However, replacing the ideal passive components with real components from SilTerra PDK deteriorates the results substantially.

Hence, a test circuit is designed by replacing the transistors of Fig. 1 with ideal sinusoidal sources as shown in Fig. 2. The purpose of the test circuit is to investigate whether the balun and the series capacitor C_S provide the required impedance transformation and phase shift, respectively, when real components are employed.

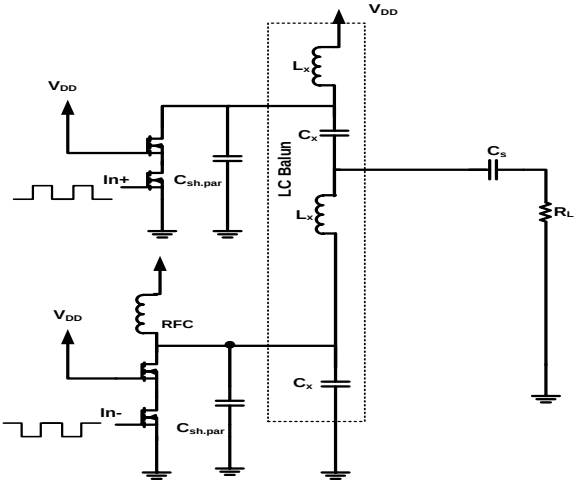


Figure 3 Schematic of differential Cascode Class-E PA with RF Choke

Simulations on the test circuit indicate that the major disturbance is caused by the parasitic components of inductors in SilTerra PDK (real inductors). The inductor model contains parasitic capacitance and resistance in addition to the desired inductance.

This leads to unanticipated behavior of the balun and a mistuning effect due to which the phase shift required for Class-E operation is disturbed. Thus, as an intermediate step, semi-real inductors (ideal inductors with a finite quality factor) are used to simulate the circuit's behavior with inductors' parasitic resistance only. This approach yields much feasible results:
First harmonic output power = 27.64 dBm
Power Added Efficiency = 34 %

The balun inductor and capacitor are parameterized as follows:

$$L_x = \frac{\sqrt{100R}}{2\pi f_{in}} \quad (1)$$

$$C_x = \frac{1}{2\pi f_{in}\sqrt{100R}} \quad (2)$$

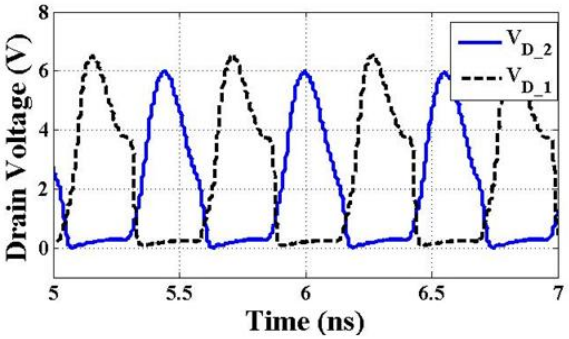
where, the parasitic resistance for L_X is:

$$R_{parasitic} = \frac{\sqrt{100R}}{Q_s} \quad (3)$$

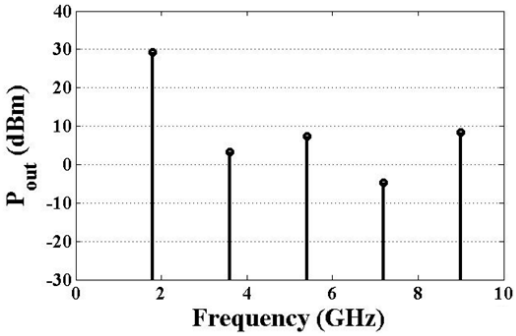
The L-C tank values (for L_0 and C_0) have been parameterized as follows:

$$L_o = \frac{50\left(1+\frac{1}{\sqrt{2\pi f_{in}\times 50C_s}}\right)}{Q_p\times 2\pi f_{in}} \quad (4)$$

$$C_o = \frac{Qp}{50\left(1+\frac{1}{\sqrt{2\pi f_{in}\times 50C_s}}\right)2\pi f_{in}} \quad (5)$$



(a)



(b)

Figure 4 Simulated results for Class-E PA (with RFC) using real passive components
(a) Drain voltage transient waveform
(b) Output power spectrum

where the parasitic resistance for L_O is:

$$R_{parasitic} = \frac{2*\pi*f_{in}*Lo}{Qs} \qquad (6)$$

Major power loss in this scheme is due to the fact that the DC path for second arm of the differential amplifier consists of two series inductors which offer a huge parasitic resistance. Hence, an alternative approach for providing the DC path is used i.e., an RF Choke (RFC) inductor directly connecting the second arm to the DC power supply, as shown in Fig 3.

At this stage, real passive components are employed using the RF Choke approach which improves the results substantially:

First harmonic output power = 29.31 dBm
Second harmonic output power = 3.24 dBm
Power Added Efficiency = 51.75 %

Fig. 4(a) shows voltage waveforms at the drains of the Common Gate transistors and Fig. 4(b) shows approximately 29.31 dBm output power at 1.8 GHz. These results are obtained using the following component values: V_{DD} = 2.5V, C_S = 2.4pF, Q_S = 16, L_{RFC} = 3.6nH, Q_{RFC} = 30, R = 8Ω, R_L = 50Ω, L_X = 2.5nH, C_X = 3.126pF, W_{CG} (Width of Common Gate transistor) = 6mm, W_{CS} (Width of Common Source transistor) = 4mm.

B. Driver Stage – a CMOS Inverter Chain:

Class-E power amplifier is a switching amplifier

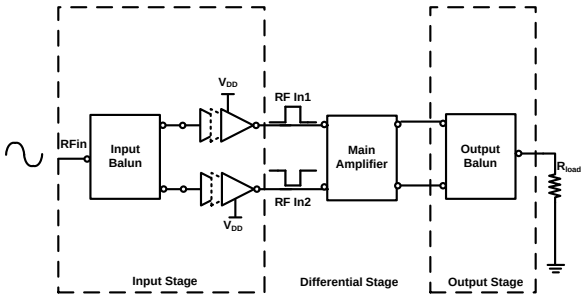


Figure 5 Block Diagram of Complete Amplifier Design

which requires input pulses with sharp rising and falling edges for its efficient performance. Generally, modulated RF sinusoidal signals are provided as input to RF amplifiers. However, for switching amplifiers, the sinusoidal signal is converted into rectangular pulses by cascading a driver or input stage with the main amplifying stage as shown in the Fig. 5.

The input stage consists of an input balun, a buffer stage and an inverter chain. The input balun is be placed off-chip to provide a differential input to the design. The buffer converts the input sinusoidal signal into rectangular pulses of the same frequency and phase. It consists of two same-sized CMOS inverters. The first buffer stage is given a gate bias for having the desired duty cycle of the input pulses.

The rectangular pulses from the buffer stage are fed into the inverter chain. The CMOS inverter transistors work in complementary fashion and produce rectangular voltage signal. A chain of inverters with tapered transistor widths is used instead of a single inverter. This is because the differential power amplifier design has very high capacitance at the input which requires high current from the driving stage [4].

The following results are obtained after including the driver stage in the schematic:
First harmonic output power = 29.2 dBm
Second harmonic output power = 4.49 dBm
Power Added Efficiency = 47.1 %

III. LAYOUT DESIGN

Fig. 6 shows the final layout design of the Class-E PA. Octagonal shaped planar inductors are used since **s**quare-shaped inductors produce antenna effect and can immensely deteriorate the performance of the design. Asymmetrical inductors have been employed as they offer high quality factor as compared to symmetrical inductors.

The design proposes that Bond Wire inductance will be utilized for providing RF Choke of high quality factor. Therefore, a bond pad has been reserved for the bond wire inductor (RFC).

IV. RESULTS

Post layout simulation is performed after back-annotating the schematic with extracted parasitic values

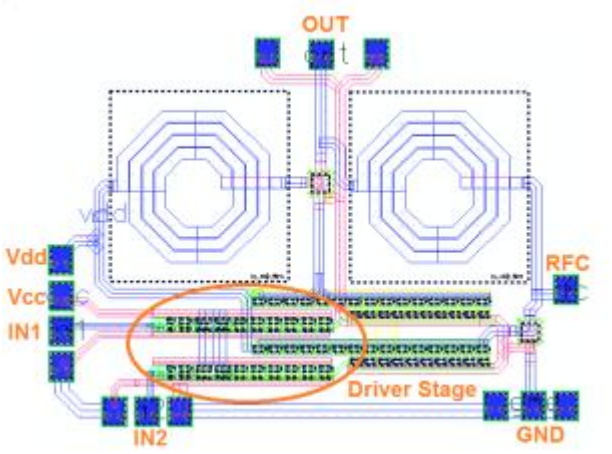


Figure 6 Layout Design of Class-E PA

and the following results are achieved at 1.8 GHz:
First harmonic output power = 26.8 dBm
Second harmonic output power = 3.35 dBm
Power Added Efficiency = 38.9 %

SilTerra offers some noteworthy technology features like built-in Electrostatic Discharge (ESD) protection for bond-pads, Circuit Under Pad (CUP) technology, triple-well transistors and high quality-factor asymmetrical inductors.

Maximum width of a single transistor is 640um in SilTerra's PDK while IBM allows transistor width up to 1mm. Moreover, punch-through breakdown voltage of transistors in SilTerra is substantially less as compared to those in IBM's equivalent technology.

Customer support from SilTerra has not been satisfactory and has caused significant delays in design completion.

V. CONCLUSION

In this paper, a differential cascode Class-E power amplifier is discussed which is successfully designed using SilTerra's 130nm CMOS technology. This proves that the technology is capable of being used for demanding RF applications. The pitfalls observed during the optimization phase and the strategies used to mitigate the parasitic effects are also described. The flexibility provided by SilTerra in layout design and the unique technology features are highlighted which assist in designing compact, reliable and power-efficient ICs. Some areas of improvement have also been identified which can enable SilTerra to perform even better in the global semiconductor industry.

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