# Design 1-bit full adder and Comparative Study of Different Type of Adders in terms of Power Consumption, Area and Delay

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***Abstract:*** In this paper a new design of 11T 1-bit full adder has been proposed. It is compared with different 1-bit full adders. By using this adder as a building block we can perform arithmetic operation efficiently because adder is one of the important components of digital system applications. Microwind tool is used for simulations purpose. This paper presents mainly the pertinent selection for choosing different types of adders. The evaluation is done on the basis of performance parameters which are Area, Speed and Power Consumption. Adders are extremely imperative in majority of DSP applications and in control systems. So the precondition of the adders is that they should be speedy and competent in terms of power consumption and chip area. The adder topologies are carry look-ahead adder, carry skip adder, carry select adder and ripple carry adder.

***Keywords*****:** nMOS, pMOS, X-OR, PDP, carry look-ahead adder, carry skip adder, carry select adder, ripple carry adder**.**

## I. INTRODUCTION

In the era of huge amount of portable electronics devices, the low-power consumption and area are most important. The general trend is that the frequency and circuit complexity is increasing in order to occupy the fast and portable electronics devices. Adder is the essence of all arithmetic operations like subtraction multiplication and division. Addition is performed in most of vlsi applications like FPGA, processors. So keeping in mind to make a fast and efficient electronics system it is necessary to make the full adder as efficient as possible.

In numerous computer processors, adders are used not only in arithmetic logic unit (ALU) but also in other parts of processor, where they are used to evaluate table indices, addresses and alike operations. Addition typically impacts extensively the overall performance of digital and control systems and critical arithmetic functions. Adders are used to erect multiplies. Millions of instructions are executed per second in microprocessor, so speed of operation is vital as designing multipliers. The ample progress in the field of portable systems and cellular networks has intensified the research pains in low power microelectronics. So, low power design also has turn out to be a major design concern. In this paper we make the comparison of 11T proposed 1-bit full adder with 10T, 11T full adders which in terms of power area and delay. Already proposed full adder may have less number of transistors but may have disruptive output. So we scarify only few transistors to have precise results.

There are many different adder architectures for speeding up binary addition have been proposed over the last decades.
Carry look-ahead offers rapid speed but it consumes more area as it has O(log(n)) delay and O(n.log(n)) area, but it usually undergo from irregular layout. There is no fan in/out limit in Carry look-ahead Adders. Ripple Carry Adder exhibits the most compact design, but slowest adder with O(n) delay and O(n) area. Carry Skip Adder and Carry Select Adder act as the compromise between the two adders with O(n) area and $O(n^{l+2/l+1})$.

In this paper section II presents the previously proposed 10T transistor that had some degraded output then we discussed about 11T 1bit full adder which has one extra nmos as 11T, finally this section presents the new proposed 11T transistor which has pmos as 11T. In section III presents the different types of adders. Section IV presents all the circuit

simulation result by using Microwind software. In section V gives the conclusion of this paper.

## II. M0DELS OF 1-BIT FULL ADDER

In this section, different 1-bit full adders have been discussed.

### A. 10T 1-BIT FULL ADDER

10T 1-bit full adder is shown in fig below, which has two inputs A and B. Two outputs Sum and Cout. High voltage supply $V_{dd}$ to take as high or "1". This circuit gives all the result accurate when our input B=1.

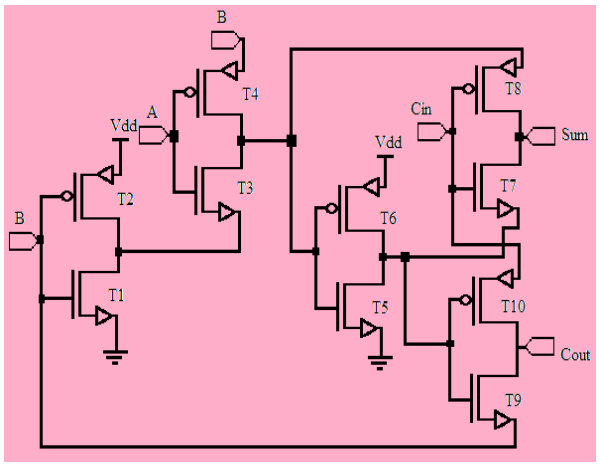


Fig. 1 Circuit diagram of 10T 1-bit full adder

Consider when input B=1 and A=0 then T1 and T4 are on. T4 passes $V_{dd}$ or "1" because pmos passes strong 1 and T1 pass "0" because it is an nmos and it pass strong "0" without loss. Then input goes to T5 and T6 as input. If input is not degraded and high "1" then T5 which is an nmos becomes on and passes strong zero and if input is low "0" then T6 which is a pmos becomes on and passes strong "1". Now consider the next case when B=1 and A=1 then T1 and T3 are on both are nmos and have to pass "0" they pass that 0 without any problem. The table below shows all the combinations of inputs and corresponding outputs at T3 and T4 common points.

Table 1 Combinations of inputs and output for 10-T 1-bit full adder

| **A** | **B** | **Out** |
|---|---|---|
| 0 | 0 | $V_{tp}$ |
| 0 | 1 | $V_{dd}$ |
| 1 | 0 | $V_{dd}$ - $V_{tn}$ |
| 1 | 1 | 0 |

We observe that when B=0 than there is loss either by an amount of $V_{tp}$ or $V_{tn}$ at the common output of T3 and T4. When B=0 and A=0 then T2 and T4 are on.T4 which is a pmos have to pass 0 but we know that pmos is not a good switch to pass 0, it degraded output by an amount $V_{tp}$ .When B=0 and A=1 then T2 and T3 are on. T2 passes $V_{dd}$ which goes at the input of T3 which is a nmos pass strong 0 and degraded 1 or $V_{dd}$, now T3 has to pass $V_{dd}$ so it gives $V_{dd}$ – Vtn. So these degradation leads to wrong results.

### B. 11T 1-BIT FULL ADDER

This circuit consists of one extra nmos transistor to increase circuit performance. By using one extra transistor the loss in V by either an amount of Vtp or Vtn as in 10T full adder has been removed. When both the input signals are low then T11 nmos try to pass zero without less loss. In this 11T full adder the power consumption is decreased to a great extent at the cost of small area over head. [6]

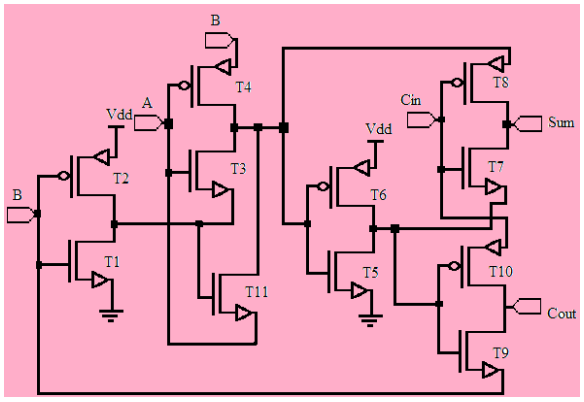


Fig. 2 Circuit diagram of 11T 1-bit full adder

But the disadvantage of using extra 11T is the area increased and nmos passes strong 0 but degraded 1 that's why there is advantage only when B=0 and A=0 but not such an advantage when B=0 and A=1 because it degrade $V_{dd.}$ The table below shows all the input and corresponding outputs at T3 and T4 common point.

Table 2 Combinations of inputs and output for 11-T 1-bit full adder

| **A** | **B** | **Out** |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $V_{dd}$ |
| 1 | 0 | $V_{dd}$ - $V_{tn}$ |
| 1 | 1 | 0 |

## C. PROPOSED 11T 1-BIT FULL ADDER

In this circuit one extra transistor T11 which is a pmos is connected to get the accurate output. As in the previous 11T 1 bit full adder there is degradation in output when A=1 and B=0, to remove this error we proposed the new 11T 1 bit full adder which has the same number of transistors but better performance.

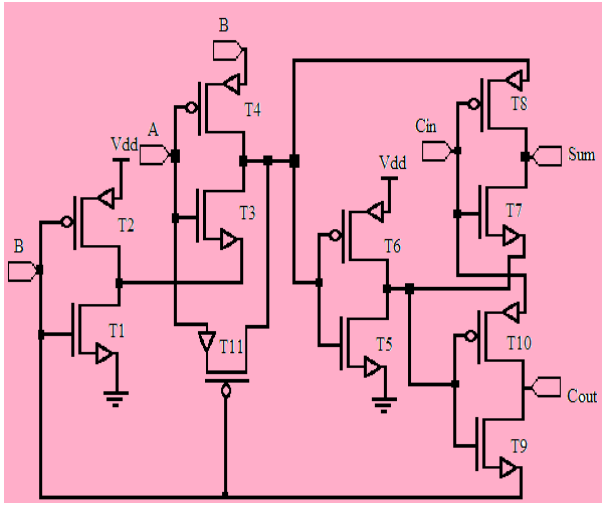


Fig. 3 Circuit diagram of proposed 11T 1-bit full adder

When input B=0 T11 is on and it passes the vale which at the input A. We have the problem with previous circuit when B=0 and A=1, in this case T11 passes A=1 at the output Vdd without any degradation and supports T4 when A=0. So this 11T which is a pmos strongly pass the 1 which means $V_{dd}$ is passes without loss.

## III. DIFFERENT TYPES OF ADDERS

This section describes the functioning of different types of adders when number of adders has been concatenated.

## A. CARRY LOOK-AHEAD ADDER

Engineers devised faster ways to put in two binary numbers by using Carry Look-ahead Adder in order to decrease computation time. Carry look-ahead adder is introduced to prevail over latency due to rippling effect of carry bits. Less number of gates is used in CLA. The Carry look-ahead Adder (CLA) improves speed by tumbling the amount of time required to determine carry bits. CLA use concept of generating (G) and propagating (P) carries. Its work is based on two signals called p and G for each bit position. The P and G are given as:
Ci+1 = Gi + PiCi where Gi =AiBi and Pi= Ai ⊕Bi

$$Si = Ai \oplus Bi \oplus Ci \quad (1)$$

By mingling multiple carry look-ahead adders, even larger adders can be formed. That can be used at multiple stages to create even larger adders.

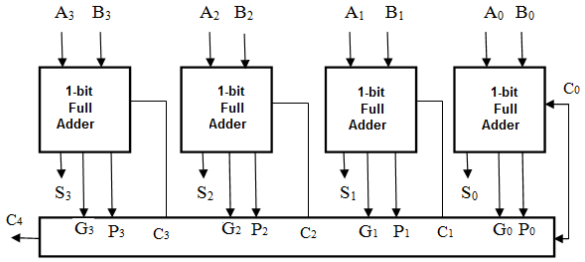


Fig.4 Block diagram of 4-bit Look-ahead Carry

## B. RIPPLE CARRY ADDER(RCA)

Concatenating the several full adders to add N-bit numbers form a Ripple Carry adder. This is called Ripple Carry Adder because every carry bit ripples to the next full adder.The arrangement of RCA is trouble-free, which permit for fast design time. On the other hand, the ripple carry adder is

comparatively slow, since each full adder must stay for the carry bit which is coming from the preceding full adder, it tranverses longest critical path so show worstcase delay. The equations for RCA are:

$Ci+1 = Ai\ Bi + (Ai + Bi)\ Ci$ (2)

$Si = Ai \oplus Bi \oplus Ci$ (3)

If RCA is implemented by concatenating N full adders, the delay of such an adder is 2N gate delays from Cin to Cout.

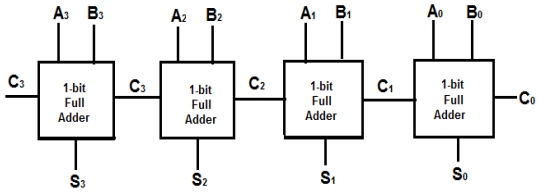


Fig.5 Block diagram of Ripple carry adder

## C. CARRY SKIP ADDER(CSKA)

Carry Skip adder needs less area and consumes less power. A Carry skip adder divides the words to be added into froup of equal size. Carry Skip adder consists of a simple ripple carry adder with a special speed up carry chain which is known as skip chain. When addition of large number of bits is required, then Carry Skip adder is better than ripple carry adder. Ripple Carry adder is suitable for small number of bits, however in present most computers use 32 bit word length, so Carry skip adder is suitable these days. It has simple and regular layout along with less delay. In CSKA, adders of N stages are divided into stages of selected lengths with simple Ripple Carry.in each group, the group carry will propagate if $p_i$ =1 in every group. The carry in bit in the case of CSKA is designated as $C_{in}$ and the output carry is designated as cout. Each adder also produce a carry-out bit. The circuitry of CSKA consists of two lodical gates i.e AND gate and OR gate. The AND gate performs operation on $C_{in}$ and campares it with group propagate signals.

$P_{(i,i+3)} = P_{i+3}.P_{i+2}.P_{i+1}.P_i$ (4)

Using the individual values, the output from the AND gate is ORed with $C_{i+4}$ to produce a stage output of

$Carry = C_{i+4} + P_{(i,i+3).}\ C_i$ (5)

If $P_{(i,i+3)} = 0$, then the carry-out of group is determined by the value of $C_{i+4.}$ But if $P_{(i,i+3)} = 1$, then the Carry-in bit is $C_i = 1$,then group carry will propagate to next group.

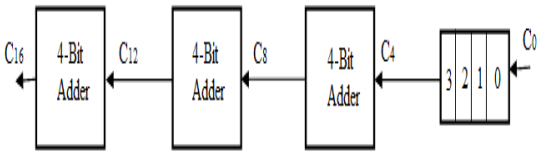


Fig.6 Ripple carry adder

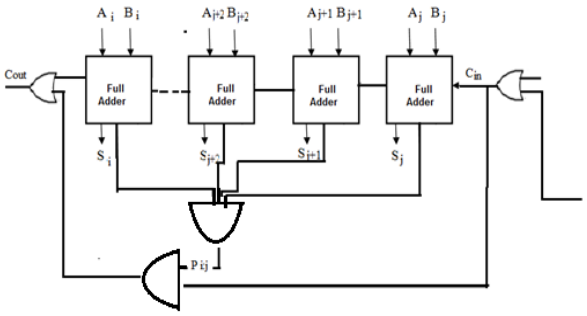


Fig.7 Block diagram of Carry skip adder

## D. CARRY SELECT ADDER (CSA)

Carry Select Adder comes in the category of conditional sum adders. It is divided into two sections, each of which perfume two additions in a parallel way, one with carry-in of zero and other with carry-in of 1. A four bit Carry Select adder consists of two ripple carry adders and a multiplexer. The Carry select adder consists of k/2 bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits two k/2 bit adder. The carry out calculated from least significant bit stage selects the actual value of output carry and sum. In most significant stage, one addition is performed by taking carry as zero and other by taking carry as 1. This technique cause to increase area but operation of addition is very fast here.

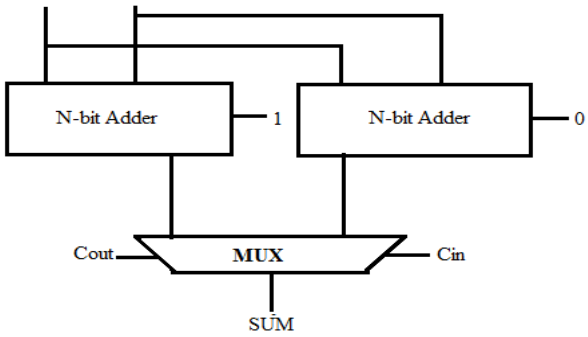


Fig.8 Block diagram of carry select adder

## IV. SIMULATION

The above circuits are simulated in Microwind software and we observe that the last circuit has the less delay and improved efficiency.

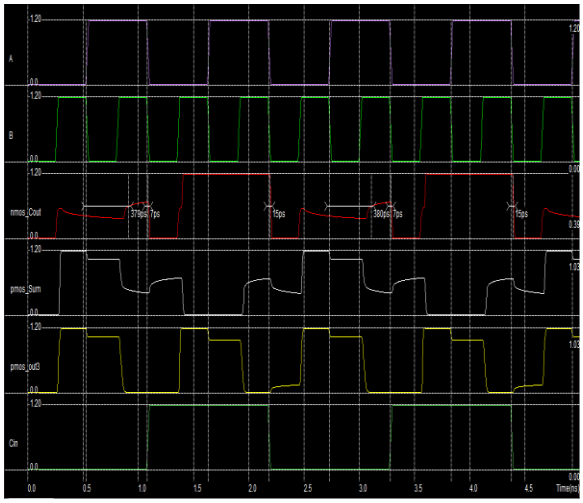

Fig.9 10T full adder simulation result

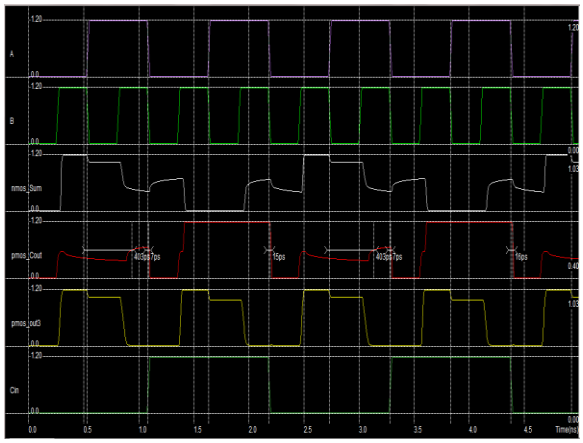

Fig.10 11T full adder simulation result

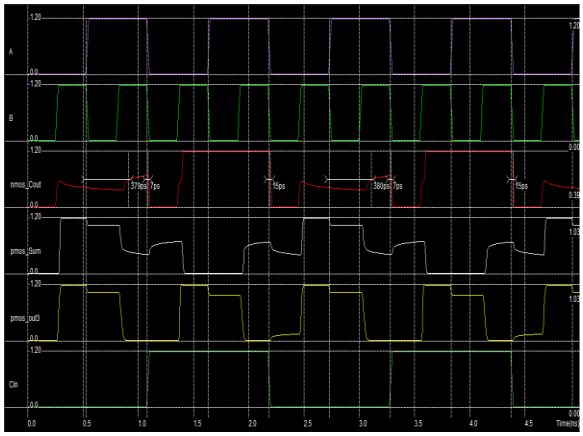

Fig...11 Proposed full adder simulation result

From the above results we see that the proposed full adder has the less delay compared to 11T full adder and same performance. Comparing with 10T full adder it has approximately the same delay and performance is much improved than 10T full adder.

## V. CONCLUSION

We observed that power PDP has been reduced by scarify only one transistor. We get the accurate output than the degraded. It also has temperature stability then the existing one full adder. So we can use this circuit for low power applications. Because adder is the basic most building block for of the circuits so increasing this basic unit performance we improve our complex circuit by noticeable amount.

We discussed four types of adders on the basis of performance. Different adders can be used in different applications according to the requirement of application. But Carry Skip Adder and Carry select adder are best one

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